ALICE Trigger System

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Abstract

The ALICE Trigger System is made up of two independent parts: a Central Trigger Processor (CTP) and a Trigger Distribution Network.

The CTP provides the trigger decision logic. It generates triggers for the readout detectors by evaluating inputs from triggering detectors.

The Trigger Distribution Network delivers these triggers to the detectors; in addition it is capable of running in standalone mode, which enables independent testing and calibration of detectors excluded from the global run.

A brief overview of both parts is presented, focusing on the latest developments in building and testing the Trigger Distribution Network.

I. INTRODUCTION

The trigger development in the ALICE experiment has advanced significantly in the last year. In 2003 the CTP User Requirement Document and Preliminary Design Review of LTU wre approved. In this year, the LTUboard was developed and delivered allowing the independent development of FE electronics for particular detectors.

II. CTP LOGIC

The CTP logic is defined by specification of the set of inputs, the set of outputs and the rules describing relations between them. The whole CTP logic is described in [5]. It can be seen as a set of Classes and Clusters as shown on Figure 1.

One Class includes the group of Trigger inputs. The Cluster consists of several Classes on its input and groups the similar triggered detectors into one group on its output. A Class becomes active, if all the inputs belonging to it are active (a logical AND of input signals). A Cluster becomes active if there is at least one of its classes active (logical OR of outputs coming from its classes). An active Cluster sends corresponding trigger signals to its detectors.

The difference in the readout time of particular detectors led to the design of the three level parallel trigger system, which allows the system to read out the data from faster detectors, while slower detectors are busy with reading out the data belonging to earlier events. The first decision is made at 1.2 μs after the event (L0), L1 decision comes after 6.5 μs and L2 trigger is issued after 88 μs.

L1, L2 decisions can kill trigger signals issued in L0 time.

There are 24 inputs for L0, 20 inputs for L1 and 6 inputs for L2 level trigger.

In addition to making decision at each level, the CTP checks the events for pile-up; there are 4 past-future protection circuits shared among the configured classes. Actually, the L2 decision means 'free of pile-up' decision.

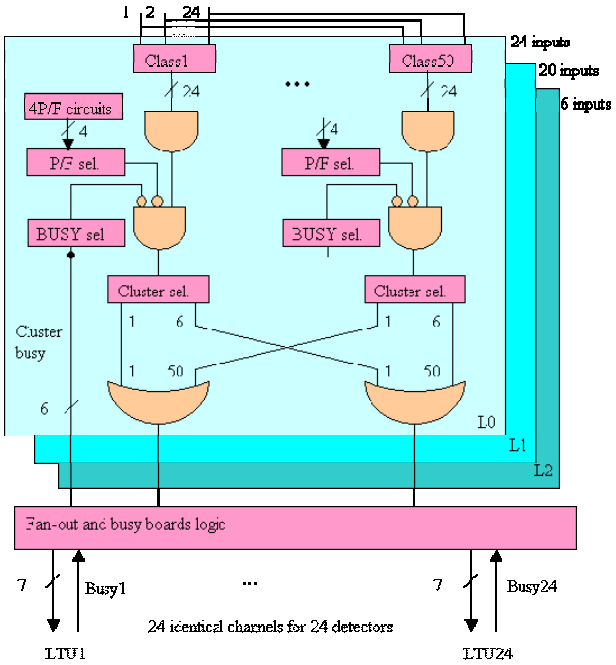

Figure 1: CTP Logic

The whole CTP logic is configured through VME interface.

BUSY logic is implemented at the L0 level. First, the input BUSY signals from each detector are grouped into

Cluster busy signals, which veto L0 signals for classes belonging to this cluster.

A similar veto is applied at L1, L2 level, but the BUSY signal is replaced there by delayed decisions from previous levels. There is a global *DAQ busy signal*, asserted by VME operation, which halts all the L0 inputs, for example so as to allow an 'on the fly' reconfiguration of the CTP logic.

III. LOCAL TRIGGER UNIT

The detectors in ALICE receive their trigger signals through a standard interface called a TTC partition in the Local Trigger Crate (LTC). The function of the TTC partition is to receive trigger signals in an internal format from the CTP and from them generate the signals required to drive the detector, using coaxial cables (L0) and the TTC system.

For a given detector, the TTC partition consists of a Local Trigger Unit (LTU) [1] and two modules (TTCvi [2], TTCex [3]) required to generate TTC signals.

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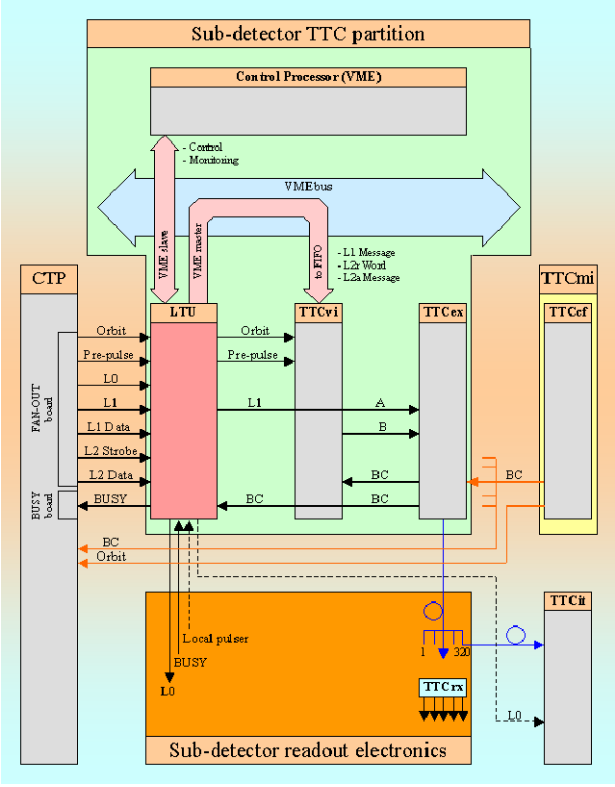

Figure 2: Context diagram for the LTU

Signals are passed between the modules in a TTC partition using the VME backplane, each LTU being the VME master and wires. The result is that there will be up to five VME masters in a single full width crate (or more if some partitions use the RoII).

The organization of a TTC partition is shown in Figure 2., where the connections both to the CTP and to the TTC components are indicated

The LTU communicates with the detector electronics, located some 20 to 50 metres away from the CTP rack, usually in the experimental cavern. The L0 trigger and the BUSY input from the detector are sent using electrical connections. All the other connections are made using signals transmitted on the TTC optical fibre. At the Front-end there are received by TTCrx chip[4].

The functions of the LTU are shown in Figure 3.

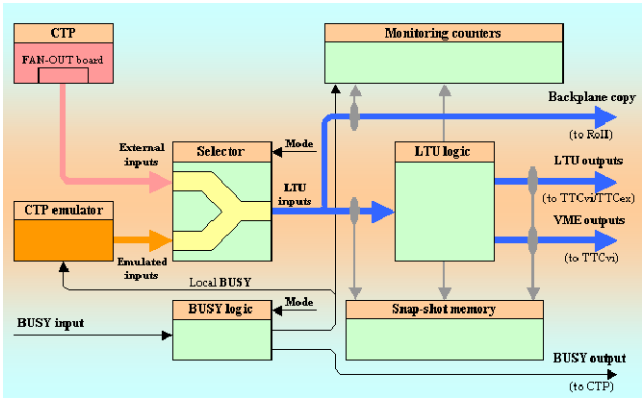

Figure 3: Block diagram for the LTU board

The board can be run in two different modes, determined by the selector. In *global* mode the LTU receives external input signals (from the CTP) which are converted to the appropriate formats to drive the TTC and/or the electrical LTU outputs. In *stand-alone* mode, these inputs are replaced by a *CTP emulator* which can be programmed to generate sequences of trigger signals. The signals are presented in an identical way to the selector block, and are then treated identically downstream of the selector. In this way, a detector governed by a given LTU receives an identical trigger environment irrespective of which mode is selected. The detector provides its BUSY signal as an input to the LTU.

In addition to these front panel outputs, which are used to drive the TTC system, there is a *backplane copy* of the same signals, sent using the user--defined pins on the VME J2 connector. The signals are provided in order to facilitate the emulation of Region--of--Interest (RoI) data in stand-alone mode.

It is foreseen that there could be a purpose--built Region--of--Interest interface board (RoII), to be placed next to the LTU for those detectors requiring RoI data, to do this. The RoII would have to be synchronized with the LTU, and this is the purpose of the `backplane copies' of the signals. In addition, these signals can be utilised for daisy-chained connection of more LTUs running in global mode, while controlled by one LTU running in standalone mode.

Monitoring facilities are provided, and there is a snapshot memory, which can record the traffic in the LTU

on a bunch crossing by bunch crossing basis over a period of some 294 LHC orbits.

The LTU performs several operations with the signals received:

- de--serialization of the L1 data and L2 data messages, and conversion to the appropriate format for TTC transmission;
- queueing and temporary storage in a FIFO of the formatted TTC words;
- control and arbitration of the FIFO read operation and transmission via the VME bus to the TTCvi board.

The data are written into the FIFO without any checks of its status. On the other hand, an external counter is used to monitor the occupancy of the FIFO, and it is prevented from overflowing by implementing a `leaky bucket' algorithm. In this algorithm, the number of words transmitted from the LTU to the TTCvi over a given interval (large compared to the transmission time for a single word) is limited to be lower than some limit, fixed in the firmware, which is chosen to be less than the number of words which can be transmitted by the TTCvi in the same period. BUSY signal is set, preventing further triggers from entering the buffer until the backlog is cleared.

IV. CTP EMULATION BY LTU

In stand-alone mode, the LTU fully emulates the CTP protocol, and enables detectors to operate independently of the CTP, at remote sites, or at times when the CTP is not available. It can emulate all existing trigger sequences. The names, structure and codes for the emulation sequences are given in Table 1.

Table 1: List of emulation sequences

Sequence name	Sequence structure	Seq. code
L0	L0	1
L2 accept	L0 – L1 – L2a	2
L2 reject	L0 – L1 – L2r	3
Calibration pre-pulse	PP	4
Calibration L0	PP – L0	5
Calibration L2a	PP – L0 – L1 –L2a	6
Calibration L2r	PP – L0 – L1 –L2r	7

A list of maximum 32 sequences to be emulated is loaded in *sequence list memory* before the start of an emulation run. The specification for each sequence, apart from sequence data, includes three control bits to indicate how the list should proceed (*last* and *restart* bits) and an *error prone* bit to indicate that the sequence is susceptible to programmable errors. The event identifier, consisting of orbit and bunch crossing number, is generated by the CTP emulator.

Each sequence is checked to see if the *last* or *restart* bits are set in the sequence list. The action of the bits is controlled by two commands given to the LTU, *break* and *quit*. If the LTU receives the command *quit* the sequence is terminated. If the control bit *restar*t is encountered, the status of the *break* command is checked. If the break command is asserted and the *last* bit is not set, the next sequence is executed. When the *break* command is set to 'no', the logic returns to the first sequence in the list.

Figure 4. shows some examples of how this may be used. The simplest case (a) is a linear sequence. Other possibilities include (b) a continuous loop, (c) a continuous loop with a subsidiary loop, and (d) a loop inside a terminating sequence.

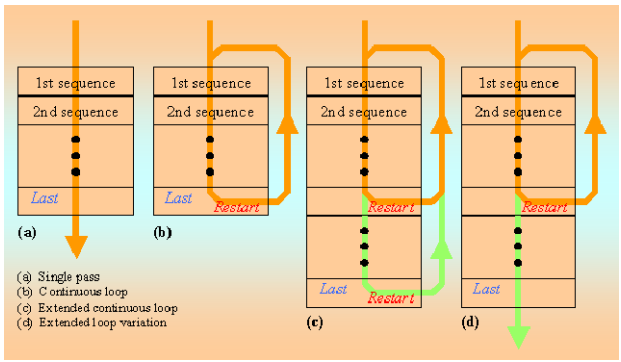

Figure 4: Example of execution patterns

The execution of sequences in *sequence list memory* is controlled consecutively by START signal, which can be generated from the following sources:

- software;
- a random signal generator, with programmable average rate;
- a scaled-down BC clock, with programmable scaling factor;
- an external pulser signal, which for example can be used to synchronize signals with a trigger in a test-beam setup.

START signal is overruled by any of the following conditions:

- the BUSY signal;
- the LHC long gap;
- if the current sequence is a calibration sequence `waiting' for the calibration slot;
- if the current sequence is an L2a/L2r sequence `waiting' for the L1 decision.

An important function of the LTU in standalone mode will be to generate sequences displaying errors in order to test error-trapping logic in the detector electronics. The error types foreseen are missing signals in a given

sequence. In order to allow errors to occur, an *error-prone* flag in the emulation sequence description file should be set. If the flag is set, the logic will check the status of control bits set by VME. There are separate bits to indicate that the corresponding signals can be omitted, each controlled by a common error signal generated by a random signal generator with a programmable rate. These bits are ignored if the error-prone flag is not set. A second circuit of the same type activates the production of a fraction of errors for when the LTU is in global mode, as this can also be useful.

V. TESTING

The boards have been tested using external VME board for catching the data directed to TTCvi board. The output data resulting from fixed or random patterns loaded into the LTU sequence memory have been checked against LTU counters and expected values read from external board. The test setup is shown in Figure 5.

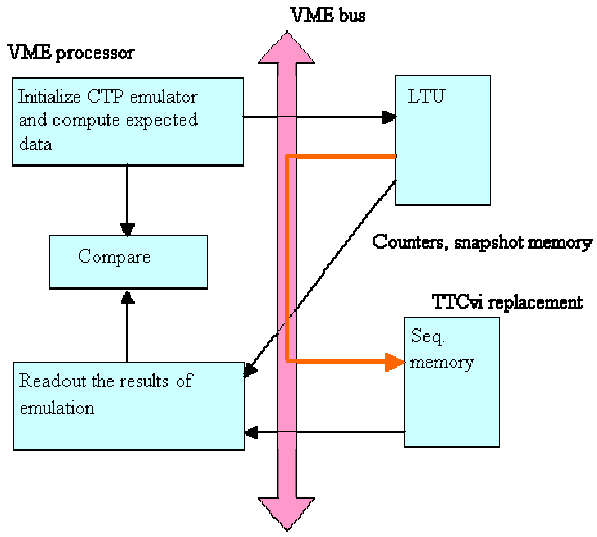

Figure 5: LTU testing

VI. SUMMARY

The requirements for the ALICE trigger ended up in 2003 with a CTP User requirement document. In this year, CTP design was presented and at the beginning of the next year the CTP is expected to be ready for testing.

In 2004, 53 LTU boards were manufactured and tested. The part of them were distributed among the ALICE experiment groups, together with the control software. The LTU boards will be used in the combined test-beam in October 2004.

VII. REFERENCES

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