The ALICE Central Trigger System

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***Abstract*- The ALICE trigger system is situated in the experimental cavern and has a *centralized* layout: the Central Trigger Processor (CTP), the sub-detector interface (Local Trigger Unit) and the TTC partitions are all installed in adjacent racks. The CTP generates *three levels of hierarchical hardware triggers – L0, L1 and L2*. At any time, the 24 sub-detectors of the ALICE experiment are *dynamically partitioned* into up to *6 independent clusters*. The level of event pile-up is controlled by the *Past-future Protection* logic.**

The Local Trigger Unit (LTU) serves as a uniform interface between the CTP and the sub-detector readout electronics. In the *stand-alone mode* of operation, the LTU *fully emulates the CTP protocol*.

An overview of the ALICE Central Trigger System will be presented, with the emphasis on the design of hardware modules.

I. Introduction

ALICE (**A** **L**arge **I**on **C**ollider **E**xperiment) is a dedicated heavy-ion detector at the CERN Large Hadron Collider (LHC). It is designed to operate in several modes with significantly different characteristics: in *Pb-Pb* mode, the interaction rate is as low as 8 kHz, but, due to the high multiplicity, the event size is very large (up to 86 MB); in the *proton-proton* mode, the event size is smaller (2.5 MB), but the interaction rate goes up to 200kHz; both the sensitivity period and the readout time of the ALICE sub-detectors vary widely and some are very long: the sensitivity period of the Time Projection Chamber is 88µs, the readout time of the Silicon Drift Detector is 260µs. More details of a general nature are available in [1].

Because it accommodates such a wide range of requirements, the ALICE Central Trigger Processor (CTP) is, arguably, the most complex among the CTPs of the LHC experiments:

- The ALICE CTP generates *three levels of hierarchical hardware triggers – **L0***, ***L1*** and ***L2***, before an event is accepted, transmitted to the Data Acquisition System (DAQ), and copied to the High Level Trigger (HLT) for further software assessments.
- At any time, the 24 sub-detectors of the ALICE experiment are *dynamically partitioned* into up to *6 independent clusters*, with an additional, software-triggered *test cluster,* configured on demand "on the fly"; the cluster configuration is fully arbitrary – clusters could be exclusive, but are more likely to overlap.
- Due to the complexity of ALICE events, a success or otherwise of the pattern recognition task is strongly dependant upon the level of event pile-up. The level is controlled by the *Past-future Protection* – a procedure that selects events with either no pile-up at all in a programmable time interval before and after the interaction, or with a number of pile-up interactions up to a programmable limit. The *Past-future Protection* operates independently for each cluster and is performed at all three trigger levels.
- Among the LHC experiments, the ALICE CTP generates the *highest data traffic over the TTC system* [8]. *Channel A* is used for transmission of the time-critical **L1** signal, in a way similar to most other experiments, but, for each trigger sequence that is confirmed at the L1 level, the following data are also transmitted *via* the TTC's *Channel B*: the *L1 Message* - 5 16-bit words; the *RoI Message* (Region of Interest option) - 4 words; the *L2a Message* - 8 words. Concurrently, in a way similar to the other systems, *Channel B* is also used for transmission of the LHC **Orbit** and of the calibration **Pre-pulse** signal.

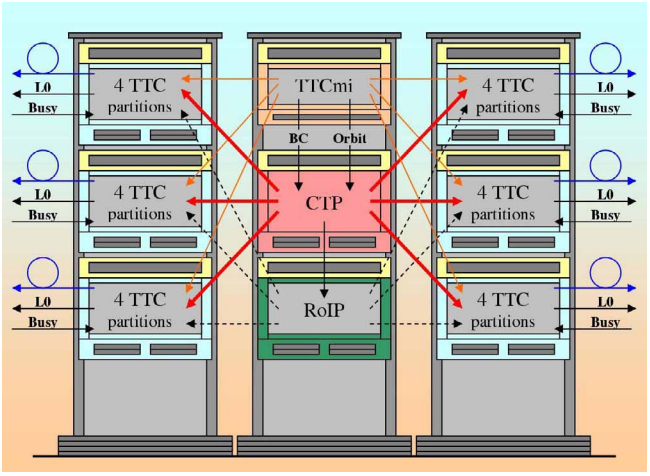

Fig. 1. Layout of the ALICE CTP in the experimental cavern

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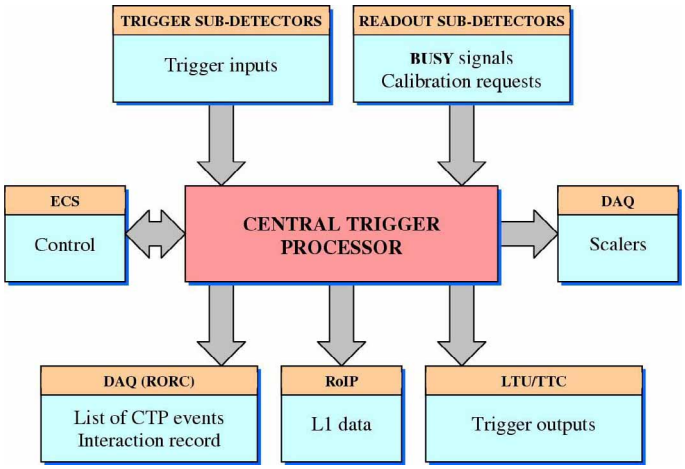

Fig. 2. Context diagram of the ALICE CTP

The ALICE trigger system is situated in the experimental cavern and has a *centralized* layout: the CTP, the sub-detector interface (Local Trigger Unit) and the TTC partitions are all installed in adjacent racks (Fig. 1).

II. Overview of the ALICE CTP

The context diagram of the ALICE CTP is shown in Fig. 2. The CTP receives and generates the following signals:

- 2 LHC timing signals (**BC, Orbit)**, from the TTCmi [5];
- 60 trigger inputs (24 **L0**; 24 **L1**; 12 **L2**), from the ALICE trigger sub-detectors;
- 24 **BUSY** inputs, one from each readout sub-detectors;
- 24 *independent sets* of 7 outputs *per* sub-detector (168 signals in total), transmitted, *via* the Local Trigger Unit and the TTC partition, to the readout sub-detectors;
- a number of signals that are part of the interface to the RoI Processor, the Detector Control System (DCS), *etc*..

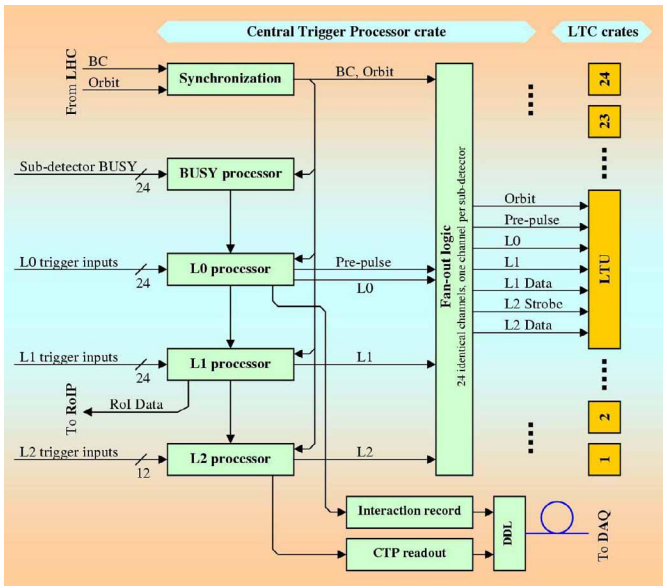

Fig. 3. Block diagram of the Central Trigger Processor

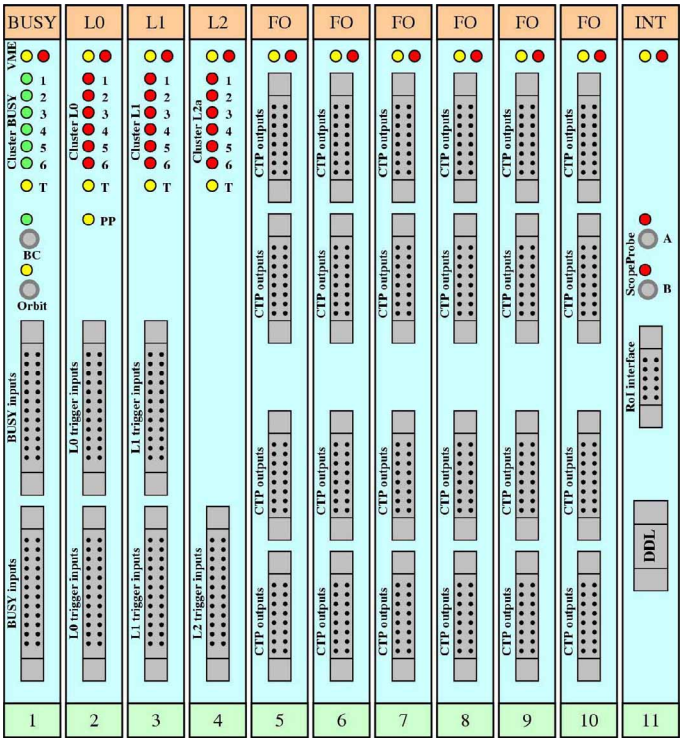

Fig. 4. The CTP VME modules and the layout

The CTP is configured and controlled by the ALICE Experiment Control System (ECS). The CTP readout provides the ALICE DAQ with detailed trigger information for each event accepted at the L2 level; the CTP also generates the *Interaction Record* – a list of all bunch-crossings in which the **Interaction** signal has been detected.

The block diagram of the CTP is shown in Fig. 3. In order to make the system modular and scalable, the functional blocks - *L0/L1/L2 processor*, *BUSY processor*, *Fan-out logic* and the *CTP interface logic* – are designed as separate VMEbus-compatible boards (L0, L1, L2, BUSY, FO and INT). The boards have a 6U form-factor, 8 PCB layers, and a moderate track and component density

The layout of the CTP boards in a VME crate is shown in Fig. 4. The CTP trigger inputs and the trigger outputs are connected *via* the front panel connectors. Connections among the boards are made over the custom backplane - a flexi-rigid circuit of 75µm thick, double-sided copper-clad Kapton film (signal tracks and ground plane); the backplane connectors plug into the VME J2, in a way similar to VME transition modules; only the user-defined pins are used; all signals are LVDS pairs; most of the data are transmitted as serial messages.

There is a lot of similarity between the CTP modules. The layout of the L0 processor, shown in Fig. 5, is a typical example of the CTP board architecture. The VME interface, the part close to the J1 connector, is controlled by the ALTERA EPM3512 FPGA. A state machine on the chip loads the configuration data into the main logic FPGA – an ALTERA Cyclone EP1C20; the data are kept in the on-board

flash memory (Am29LV081). The LVDS trigger-input receivers are close to the front panel connectors. The LVDS transceivers, adjacent to the J2 connector, buffer the board signals to the common backplane. The ADC (LTC1096L) checks the phase of trigger inputs for safe synchronization with the local bunch-crossing clock (BC). The snap-shot memory (two CY7C1382 ICs, 1M words 32-bit wide) serves to record unbiased samples of trigger inputs; during development and debugging, the memory can be used either as a source of simulated inputs, or to record output and intermediate signals in order to verify correct operation. Snap-shot memories are implemented on all the CTP boards. The PCF8591T ADC monitors all the supply voltages and the status of the fuses; the data are transmitted to the ALICE DCS *via* an independent I^2C link.

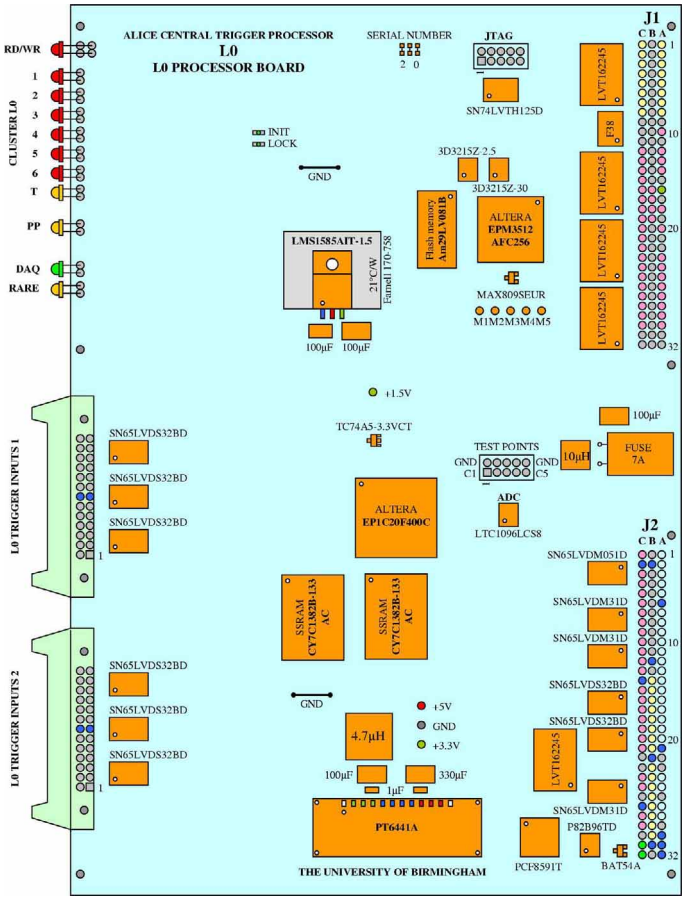

Fig. 5. L0 Processor board – the layout drawing

A. Trigger Classes and Sub-detector Clusters

The *trigger class* is a basic processing structure throughout the CTP logic. The CTP accommodates 50 independently programmable "physics" trigger classes; an additional *test class*, configured "on the fly," is triggered by the software (typical application is the calibration trigger).

A *cluster* is an internal CTP construct that significantly simplifies the processor logic; it is a programmable and unrestricted grouping of ALICE sub-detectors – clusters can be exclusive, but are more likely to overlap. The CTP supports 6 "physics" sub-detector clusters; an additional cluster is dedicated solely to the *test class*.

At any time, a cluster can be associated with an arbitrary number of trigger classes; a trigger class, on the other hand, affects only a single cluster; the association is programmable.

The generation of the Class L0 trigger is depicted in Fig. 6; the logic for the Class L1/L2 triggers is similar, but somewhat simpler. The *Trigger Condition* inputs are common to all the classes, but their application is individually programmable. The rate of class triggers can be reduced by down-scaling with a programmable factor. Programmable selection of the *Cluster BUSY* signal (one out of 6) associates the class with the cluster. *DAQ BUSY*, *CTP BUSY*, *etc*. are mandatory global vetoes. The 4 *BC Masks* are common to all the classes, but their application is programmable. The *All/Rare* signal is part of the mechanism that boosts the acquisition of "rare" events.

B. Past-future Protection Circuit

There are four independently programmable past-future protection circuits at each trigger level; an additional circuit is dedicated solely to the *test class*. A trigger class is associated with an arbitrary subset, including none; the association is programmable (Fig. 6).

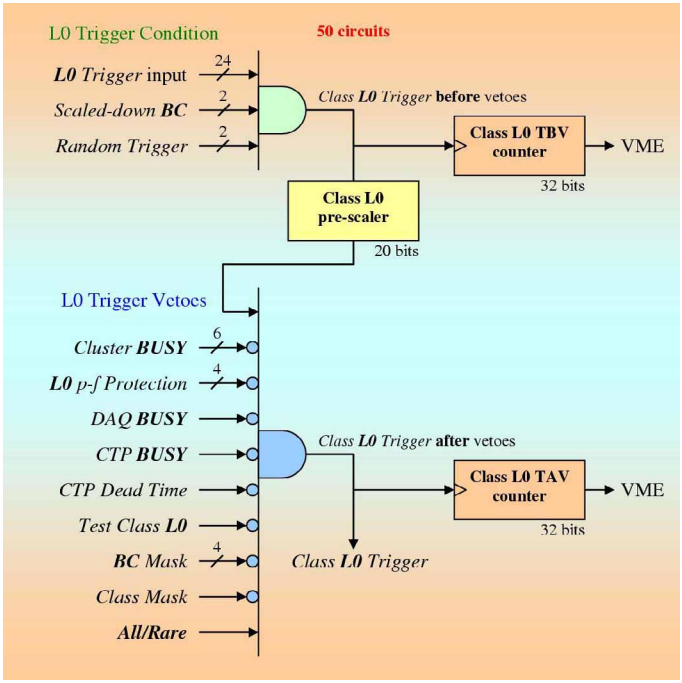

Fig. 6. Generation of the Class L0 trigger

The circuit is shown in Fig. 7. Each block generates a sliding time-window of programmable length (ΔTa/b) during which all the occurrences of the interaction signal (INTa/b) are counted; two programmable thresholds (THa1/2, THb1/2) are used to generate the corresponding outputs (Pa1/2, Pb1/2); a programmable delay serves to align the signals in time; the output P is a programmable arbitrary function of the P1 and P2

signals - the selection depicted in Fig. 7 is a typical "physics" example.

The circuit is based on a dual-port memory. A more detailed description is given in [2].

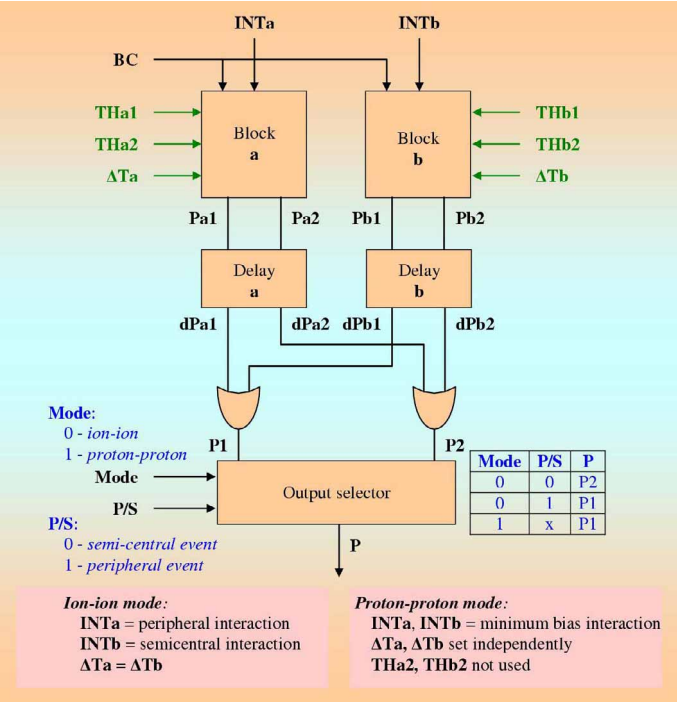

Fig. 7. Block diagram of the past-future protection circuit

III. The Local Trigger Unit

The Local Trigger Unit (LTU) [3] is also a 6U VME board (Fig. 8), in many ways similar to other CTP boards. It serves as an interface between the CTP and the sub-detector readout electronics. The existence of a uniform interface throughout the experiment greatly simplifies configuration and run-control tasks, and makes system upgrades/modifications easier to develop and implement.

The context diagram of the LTU is shown in Fig. 9. The inputs from the CTP, the time-critical outputs to the TTCvi [7] and the TTCex [6] boards, and the connections to the sub-detector readout electronics, all use the front panel connectors. The data messages (L1, L2a and L2r) are transmitted to the TTCvi FIFO *via* the VME bus; the LTU operates as a VME master; the transfer rate is regulated by the "leaky bucket" mechanism in order to prevent the FIFO overflow.

A. LTU Emulation of the CTP

In the *stand-alone* mode of operation, the LTU *fully emulates the CTP protocol* and enables sub-detectors to carry out development, test and calibration tasks independently of the CTP, at remote sites, or at times when the CTP is either not available or not required. The timing of emulated trigger sequences is identical to the timing during the *global run.*

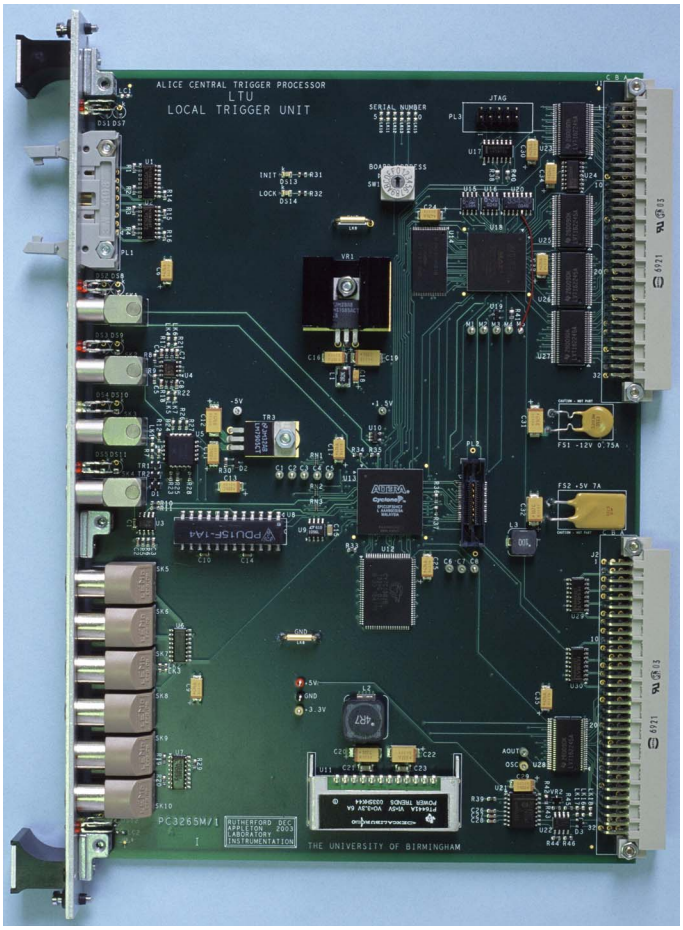

Fig. 8. The LTU board

The ALICE trigger is a *sequence*: L0 (1.2μs after the interaction) – L1 (6.5μs) – L2 (88μs). The sequence configuration depends upon trigger decisions at 3 levels. Table I lists all legal sequences; only the *L2a*/*Calibration L2a* sequence leads to the event readout.

TABLE I
LIST OF ALICE TRIGGER SEQUENCES

Sequence name	Sequence structure
L0 sequence	**L0**
L2a sequence	**L0 – L1 – L2a**
L2r sequence	**L0 – L1 – L2r**
Calibration **Pre-pulse** sequence	**Pre-pulse**
Calibration **L0** sequence	**Pre-pulse - L0**
Calibration **L2a** sequence	**Pre-pulse - L0 – L1 – L2a**
Calibration **L2r** sequence	**Pre-pulse - L0 – L1 – L2r**

The LTU emulates all the sequences; both the configuration and the content of associated data messages are fully programmable. Sequence definitions are stored in the *Sequence List* memory with sufficient capacity for up to 32 sequences (8 16-bit words *per* sequence). Sequences are executed in the order they are stored in the *List*. The sequence execution is regulated by two *sequence-flow control bits* - *Restart* and *Last*, and by two *sequence-flow commands* - *Break* and *Quit*.

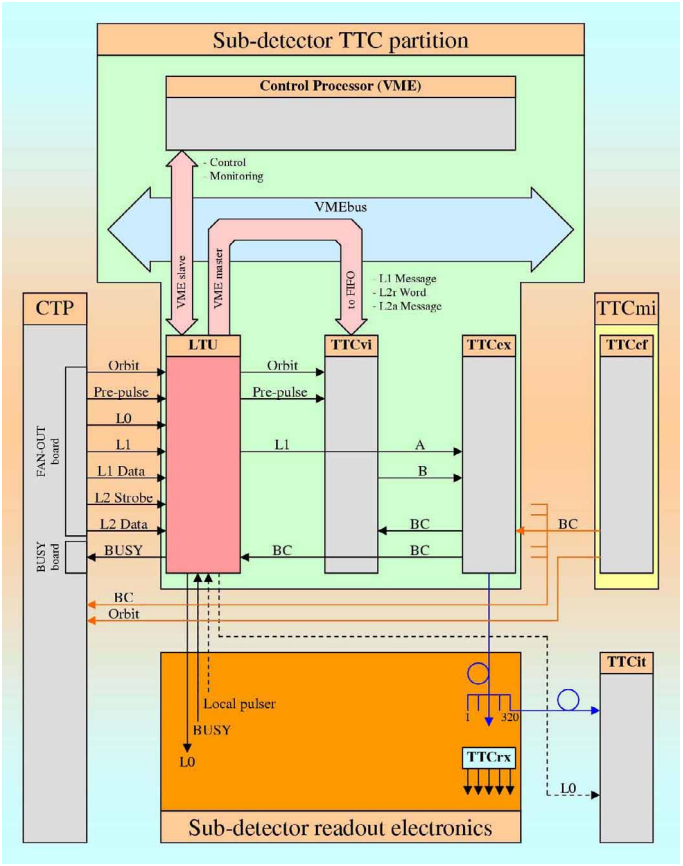

Fig. 9. Context diagram of the Local Trigger Unit

The sequence-flow options enable the execution of a number of patterns, some of which are shown in Fig. 10. The sequences from the *List* could be executed only once - *single pass* (a); or repeatedly, in a *continuous loop* (b). The exit from the loop requires the *Break* command - exit at the end of the *List*, or the *Quit* command - instant exit. The *continuous loop* is the option most frequently used. The *extended loop* (c) "adds" sequences to the main loop whenever the *Break* command is issued. The "addition" could, for example, contain the calibration sequence.

B. Error Generation

The front-end electronics of ALICE sub-detectors is required to monitor the integrity of the received trigger sequences and report the errors to the DAQ system. In order to enable the development and testing of the error-detection logic, the LTU can generate incomplete sequences, with a *fully programmable* structure. Different types of errors can be introduced either randomly - at a programmable rate, or created individually - "on demand"; the option is available in both the *global* mode and the *stand-alone* (emulation) mode.

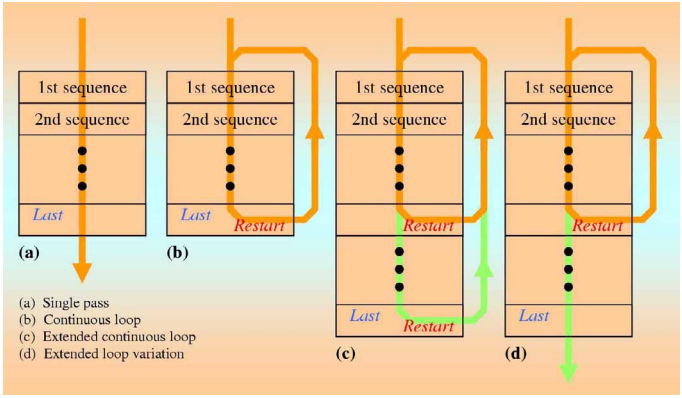

Fig. 10. Some patterns of sequence execution

IV. Status of the ALICE CTP Project

All 53 LTU boards were produced and fully tested in 2004; 23 of them were made available to the collaboration institutes to enable development and testing of the sub-detector readout electronics in proper ALICE trigger environment.

In October/November 2004, the combined beam test of the ALICE Inner Tracking System has used a configuration of 3 LTU boards as a "Central Trigger Processor." The LTUs were connected in a loop; one of them, in the *stand-alone* mode, was generating emulated sequences triggered by the beam interactions; the other two were in *global* mode, receiving the trigger signals in very much the same way as in a normal ALICE operation. The test has been the first combined use of the ALICE Trigger, the Data Acquisition System and the Experiment Control System.

All 10 FO boards have been produced and fully tested, as well as the production prototypes of the BUSY and the L0 boards; the delivery of production prototypes of the L1 and the L2 boards, and of the custom backplane are all due by the middle of July 2005; the production and testing of all 40 CTP boards will be completed during the Summer.

The installation of a complete trigger system in the ALICE experimental cavern is scheduled for the beginning of 2006.

References

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