FTT Video Conference Wednesday, Okt. 20, 1999. André Schöning

FTT L1 Design Studies

- Special code for L1 to FTTEMU added
- Starting point are D^* events from 1997
- Same L1 Scheme as shown on last meetings studied (pivot element technique)
- Synchronisation frequencies 80/20MHz used
- Valid masks are evaluated by the "fit method" (chi2 cut not optimised)

Typical Simulation Output

Printed from ufenau

SHIFT REGISTER f_synch=2			⁄IHZ	wi	th	24]	oin	S		

printout for	ievt= nsh2=	1 11	ns	gro sh2t	up= ok=		1 3	cell=	6	
P 0000000000000000 0000000000000000 00000	0000010000 1112110000 011000000 0012000000 0000100000 0010000000 100000000		$11 \\ 11 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 5 \\ 7 \\ 7$	6 6 9 9 6 9 9 9	2 2 5 2 2 2 2 5 5 5 5 5	0 0 -1 -1 -1 -1 -1 -1 -1 -1 -1				
printout for	ievt= nsh2=	1 4	ns	gro sh2t	up= ok=		1 1	cell=	5	
P 00000000000110 0000000000000000000000	00000000000 0000000000 00000000000 00000		5 5 7 7	10 10 10 10	2 5 2 5	3 3 3 3				
printout for	ievt= nsh2=	1 2	ns	gro sh2t	up= ok=		2 2	cell=	6	
00000000000000000000000000000000000000	0000002000 1111112000		0 0	3 3	7 7	0 0				

Description:	1 valid 2 valid	ma ma	ask ask	cor	rect	t 0				

Multiplicity of Valid Patterns



- overflow at 200 entries
- 70% of patterns do not include correct t0

Definition: A pattern is time invariant hit combination

Multiplicity of Valid Patterns II



- For L1 Trigger decision all patterns up to 200 have to be taken
- For Track segment finding up to 50 patterns have to be taken

Hit Multiplicities per cell



- Huge number of hit combinations to be validated
- Inclusion of adjacent hits let the number of combinations explode

Correlation hit combinations vs. hit multiplicity



- Strong correlation
- Question: should the number of hits per cell be limited?

Correlation valid patterns vs. hit multiplicity



• Possible overflows for $N_{\rm hit} > 20$

Correlation valid patterns vs. hit multiplicity consistent with BC



- Only patterns consistent with BC ($20Mhz = 2 \cdot 10MHz$)
- Number of patterns slightly reduced

Correlation valid patterns vs. hit multiplicity with correct timing included



Number of patterns reduced when t0 known

Distribution of ϕ



• ϕ is measured with respect to cell position

Distribution of $1/p_t$



• Large combinatorial backgrounds at low p_t for outer trigger groups

Correlation between ϕ and $1/p_t$



- Strong correlation between ϕ and $1/p_t$
- For trigger purposes 2*16 bins (5bits) should be sufficient for description

Resolution comparing 80MHz and 20MHz result



- plots show mainly effect of shift register granularity
- For L1 trigger purposes resolution in ϕ is sufficient
- Resolution in $1/p_t$ could be improved (necessary?)

Time depends of valid patterns



- Most patterns are valid only for 1-2 cycles and resolve BC
- Interpretation of $1/p_t$ and ϕ of valid patterns is changing drastically

Statistics



- adjacent cells have to be taken into account only for one wire per side!
- rate of combinations with correct t0 is higher for "in cell" combinations: 52% compared to 25% (priority for processing?)

Timing I



- Current simulation allows drift time differences ± 12 cycles (± 6 BCs)
- Maximum delay time to reach pivot element is 20 cycles (10BCs) plus 12 cycles (6 BCs) if using only 1 pivot element
- Only 4-5 BCs left for remaining calculations!
- Shift register could be made larger to include tails in the difference distribution but would cause additional delay

Timing II



• time distribution of all validated masks are shown for time when validation starts and when validation ends

Constraints for Design and Conclusion I

For L1 Trigger:

- 5 trigger bits for kappa and phi plus t0 indicator (1bit) to describe valid patterns
- Two 32 bit words containing the kappa-phi histogram per cell could be send to the L1 trigger card where one word contains the t0 information
- Maximum amount of all valid patterns per cell is (5+1) bit ·
 200 lines · 20 BCs = 24000 bit to be stored in an internal RAM ⇒ big FPGA
- Look Up table has to deal with about 1000 patterns without subaddresses. Amount of space is 1000 times (5+1) bit for L1 trigger · 2.5 BCs (mean value) = 21000. (still managable for all 10 BCs?)
- Design should aim for high kinematic acceptance down to low p_t than for high precision on L1 to allow triggering of $\rho \to \pi \pi$ and $\Phi \to KK$

Constraints for Design and Conclusion

For L1 track segment finding:

- additional z-information has to be processed
- κ and ϕ resolution has to be improved by using subaddress information
- track segments have only to be processed for the right bunch crossing. Can we wait so long?
- Refined track parameters have to be looked up from an external SRAM. Address defined by mask number (9/10 bit) subaddress (6 bit) and BC number (X bit) ⇒ problem?
- More studies clearly needed
- Routine to generate systematically valid patterns would be helpful