A Fast Track Trigger for H1

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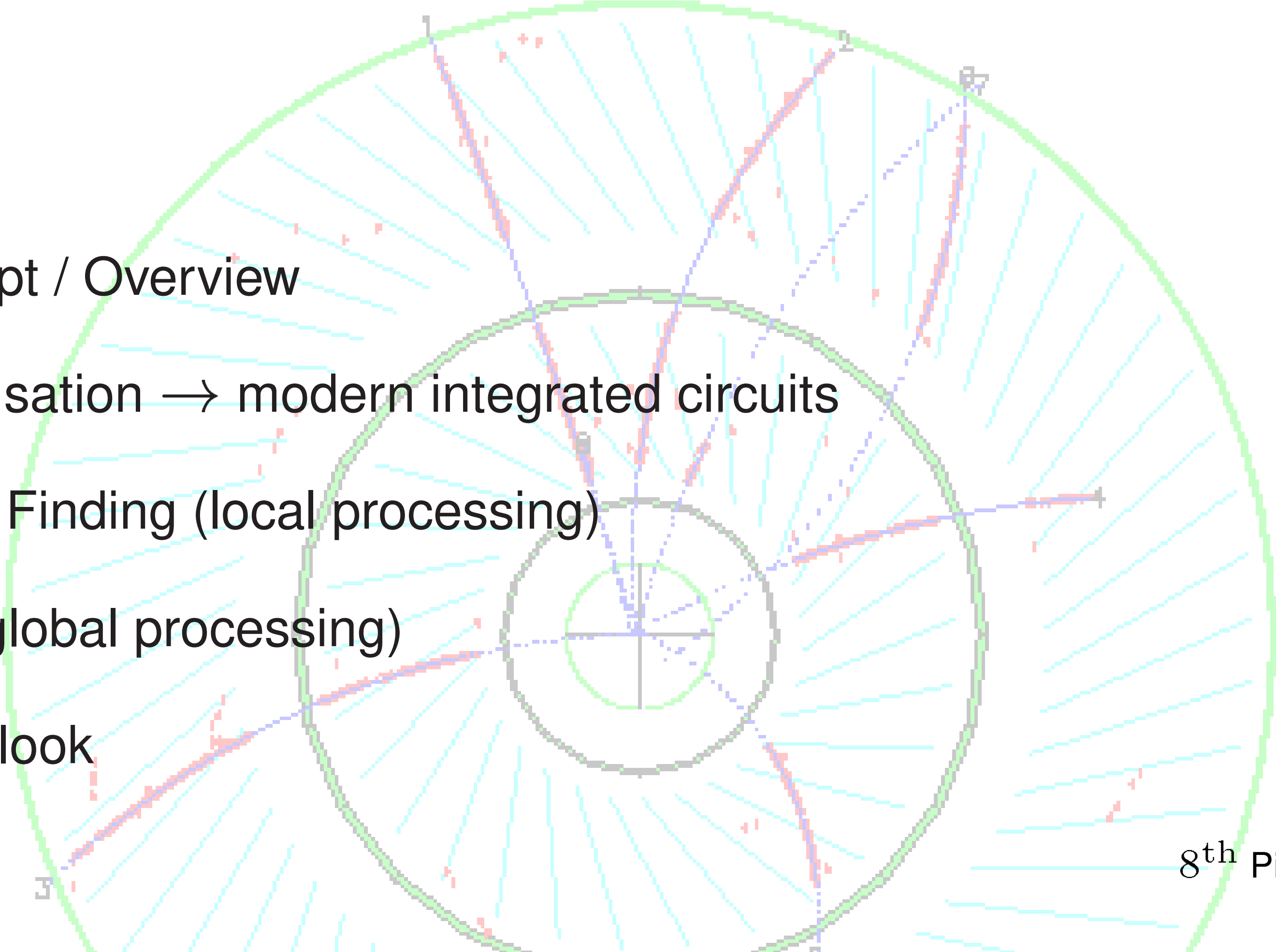
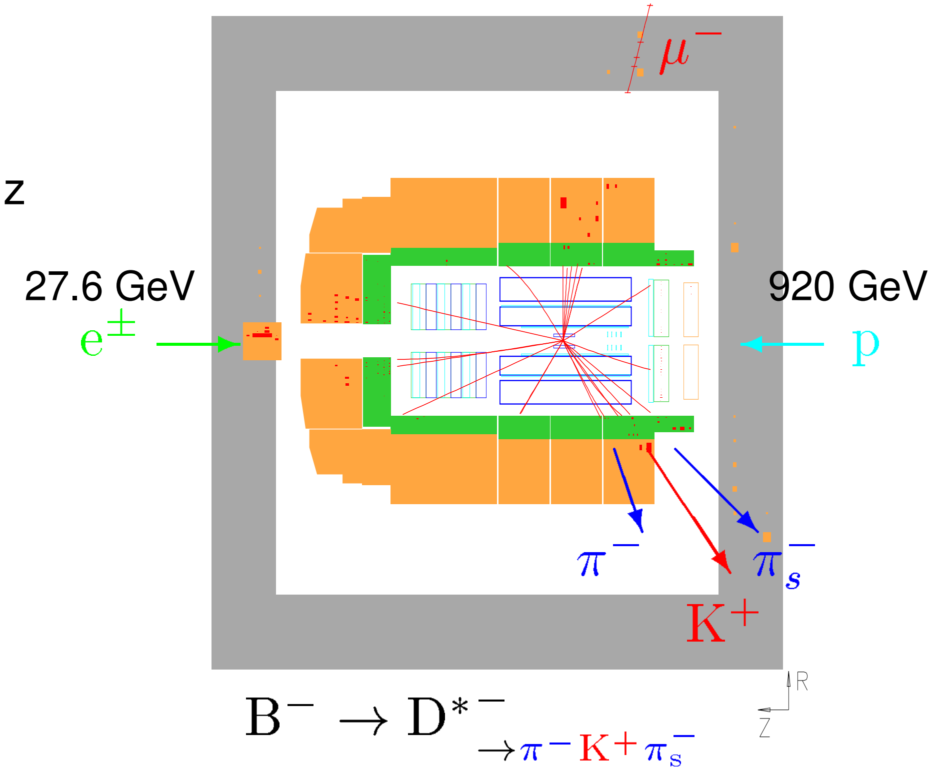


- Introduction
- General Concept / Overview
- Hardware Realisation $\longrightarrow$ modern integrated circuits
- Track Segment Finding (local processing)
- Track Linking (global processing)
- Summary / Outlook

Introduction



- HERA luminosity upgrade in 2000/2001
  $\Rightarrow$ physics rate $ep \to eX$ (DIS) of about 1 kHz
- H1 Detector
  - 4 level trigger L1-L4
  - maximum readout rate (after L3) $\approx$ 100 Hz
  - maximum logging rate (after L4) $\approx$ 10 Hz
- Events with p_t triggered by calorimeter
- Detection of exclusive final states at low p_t, e.g.

  $$ep \to eD^*_{\to \pi_s D^0} X,$$

  necessitate a new Fast Track Trigger (FTT) before full event reconstruction (level 4)
- FTT performs a track reconstruction using drift chamber hits and can identify particle decays by calculating invariant masses

FTT Specification

	existing DCrϕ (L1)	FTT (L1)	FTT (L2)
decision time	2.3 μs	2.3 μs	25 μs
topological information	2-dim. (r,ϕ)	2-dim. (r,ϕ)	detailed 3-dim.
number of drift chamber layers	8+2	9+3	9+3
hit resolution	5 mm	800 μm	300 μm
momentum range	$\gtrsim$ 400 MeV	$>$ 100 MeV	$>$ 100 MeV
track multiplicity	$N_{\mathrm{DCr}\phi} \propto N_{\mathrm{tracks}}$	precise	precise
resolution $\sigma(p_t)/p_t$ (GeV)	[0.4-0.8,0.8-∞]	0.4 p_t	0.04 p_t
z-information / inv. mass calculation	no	no	yes

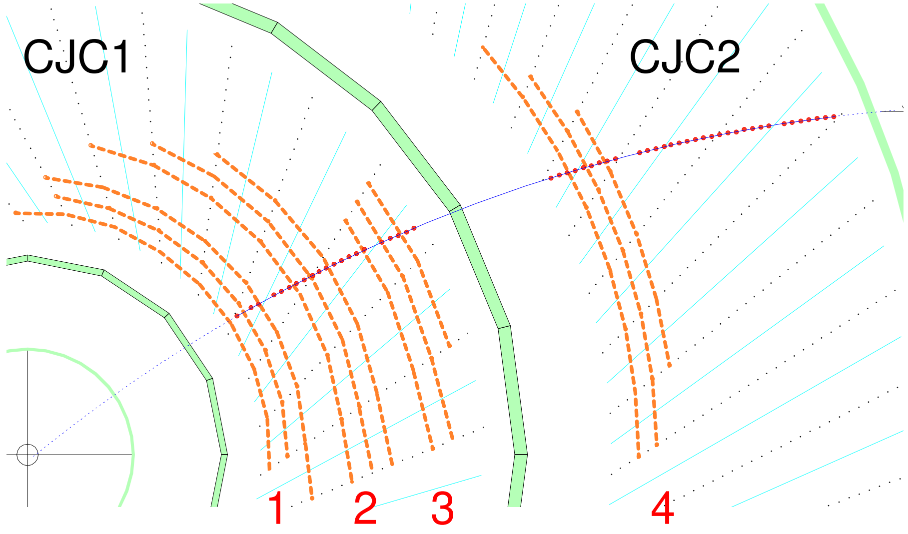
Precise track reconstruction at L2:

- up to 48 tracks/event
- up to 40000 events/sec or 2 million tracks/sec

FTT Concept

Trigger Level 1: 2.3 μs

- hit detection in 12 out of 56 drift chamber wires
- track segment finding of vertex constrained tracks in 4 trigger groups à 3 wires (1-4)



$r - \Phi$ view of the central drift chamber

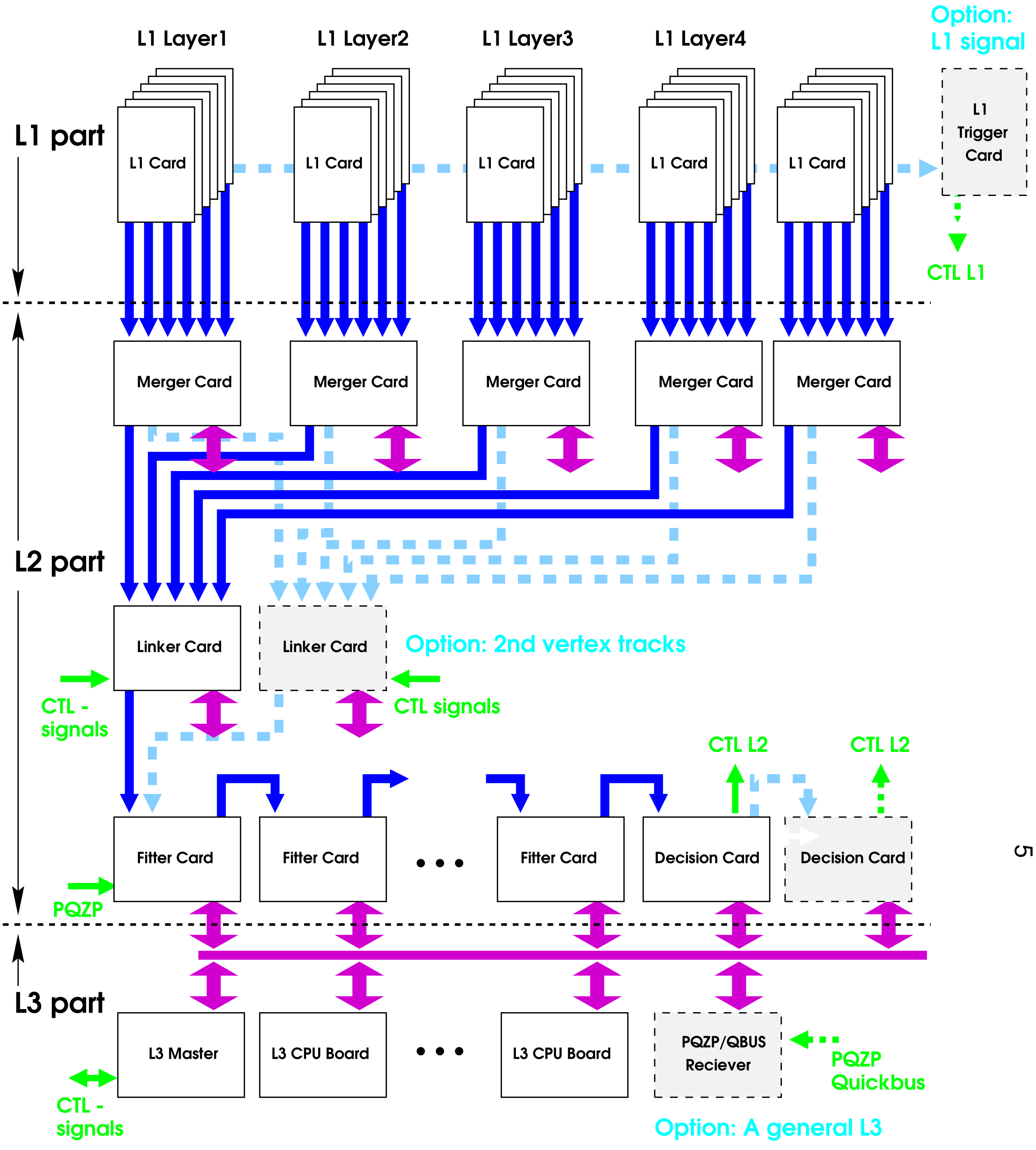
Trigger Level 2: 25 μs

- linking of track segments
- fitting of track parameters
- trigger decision from kinematic variables

Trigger Level 3: $\approx$ 100 μs

- event reconstruction and particle identification (resonances) using a processor farm

FTT Hardware Overview



LVDS: Track segments, Trackparameter

LVDS: Optional Link (2nd Vertex)

Connection to backplane

Special connections: PQZP, CTL signals

Hardware Realisation

Very demanding tasks in data processing can be realised by modern integrated circuits

- High density FPGAs (field programmable gate arrays)
  - fast with clock frequencies up to about 200 MHz
  - highly parallel with up to 1 million programmable gates
  - flexible (re-programmable)

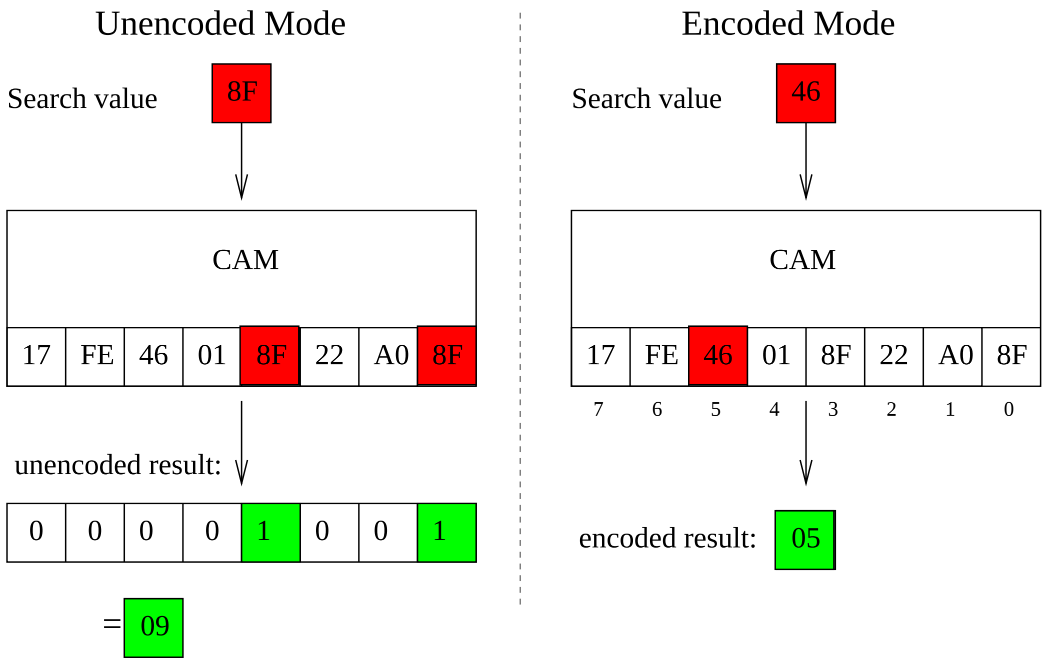
- DSPs (data signal processors)
  - fast (600-800 MHz chip announced by Texas Instruments)
  - mathematical operations
  - parallel instructions
  - flexible programming in C and Assembler

Content-Addressable Memories (CAMs)

- CAMs are inverse RAMs

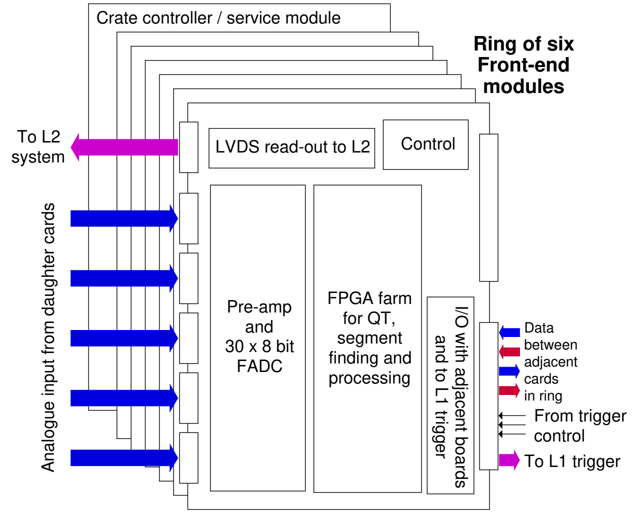
  input value $\longrightarrow$ output address

- Applications
  - networking (transform IP addresses)
  - data compression
  - search tasks in general
- Applications in HEP
  - track linking, cluster finding
  - pattern recognition, trigger



- Hardware Realisation: CAM blocks integrated in FPGAs (Altera)

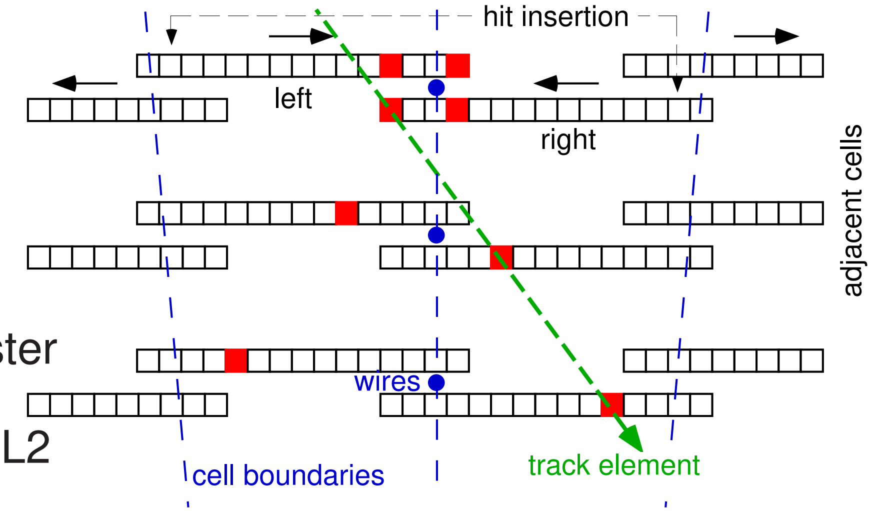
Track Segment Finding at Trigger Level 1



Local signal processing in 150 trigger groups

- digitisation using a 80 MHz 8-bit linear FADC
- hit finding $\rightarrow$ drift time + z-coordinate (charge division)
- synchronisation into shift-register (20 MHz/80 MHz)
- coarse (20 MHz) track segment validation using CAMs
  - three hit coincidence (template match)
  - rest “don’t care” bits
- L1 trigger decision based on coarse track segments (3000 types)
- refine segments by restoring 80 MHz shift-register
- send refined track segments (100000 types) to L2

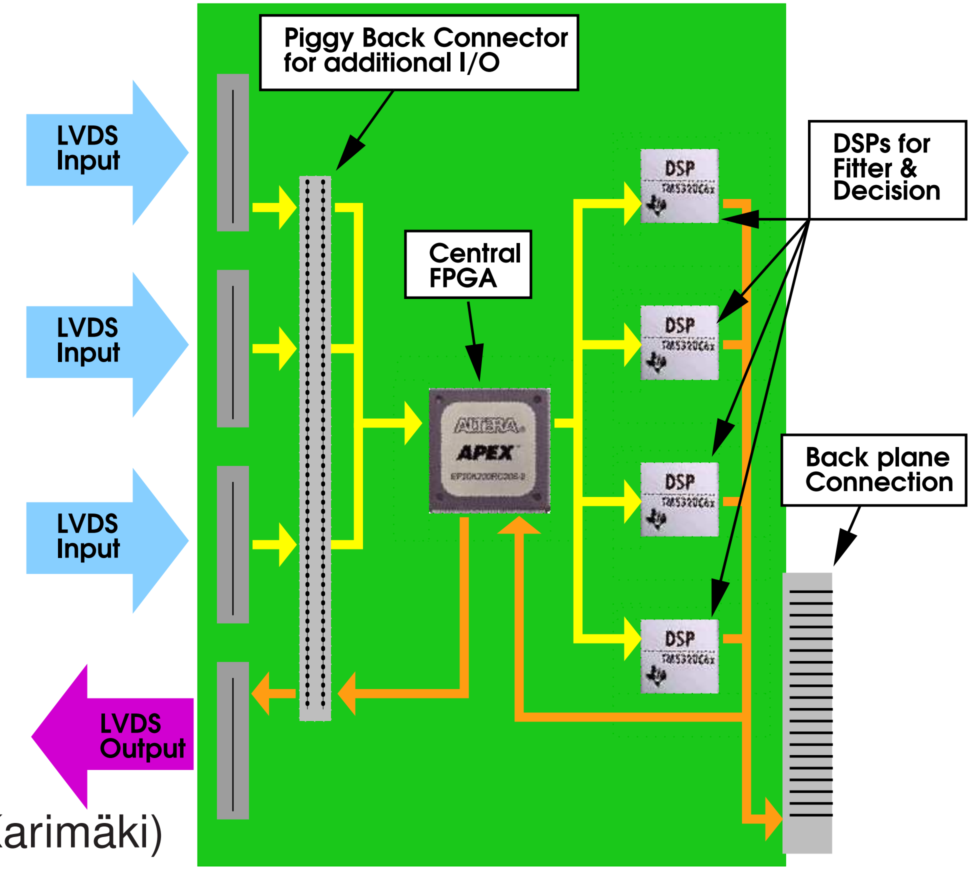
Track Segment Finding



Track Reconstruction at Trigger Level 2

Generic processing card

- merging data from L1 front-end modules
  - LVDS links
  - flexible I/O realised by piggy-back cards
- linking of track segments
  - cluster search in 2-dim $\kappa - \Phi$ histogram
  - processing $\rightarrow$ CAMs
- fitting of track parameters
  - non-iterative $\kappa - \Phi$ track parameter fit (V. Karimäki)
  - fit of polar-angle θ
  - processing $\rightarrow$ DSPs



card build in cooperation with *SCS*, Zürich

L2 Track Linking Algorithm

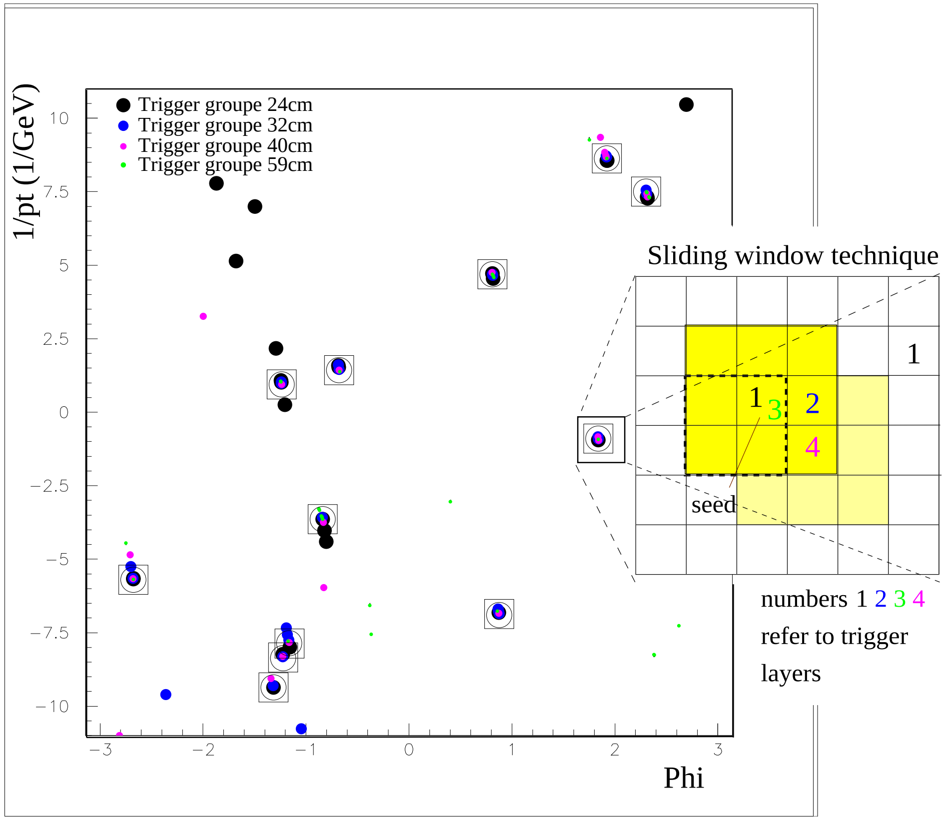
Global linking of track segments

1 Track segments are filled into $4 \cdot 25$ CAMs representing a virtual κ-ϕ histogram

2 List of track segment seeds is processed, arrays of 5×5 bins around seed are read from CAMs (1 cycle)

3 local cluster finder algorithm checks for peak position using a 3×3 sliding window (coincidence 2 out of 4 trigger layers)

- Properties of algorithm
  - few steps, algorithm is pipelined
  - highly parallel
  - total linking time $\propto$ track mulitplicity



FTT L2 Timing / Resources

task	chip	frequency	steps	max. time
receive data / fill CAMs	FPGA	50 MHz	$\leq$ 154	3.1 μs
linking of $\leq$ 512 segments	FPGA	100 MHz	$\leq$ 528	5.3 μs
fitting of $\leq$ 48 tracks	DSP	166 MHz	$\approx$ 1000	6.0 μs
trigger decision	DSP, FPGA	166 MHz	$\approx$ 500	3.0 μs
total				17.4 μs

FPGA: Altera APEX 20K600E (1 million gates)

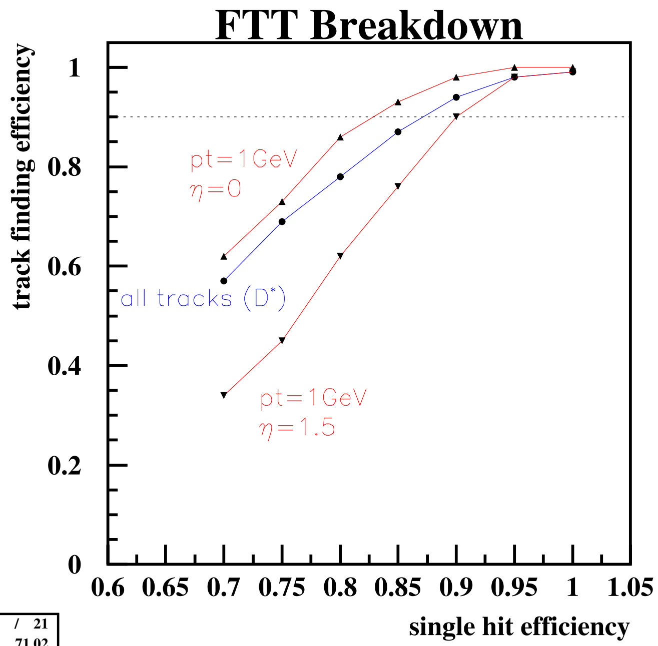
- Resources:

  128 out of 152 ESBs (embedded system blocks) mainly used for CAMs $\rightarrow$ 80%

DSPs: Texas Instruments TMS320C6701 (floating point processor)

- 48 DSPs perform track parameter fit in parallel
- faster fixed point DSPs are considered

FTT Performance

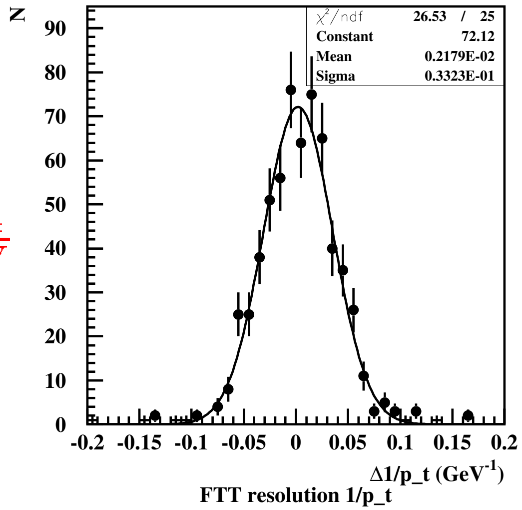


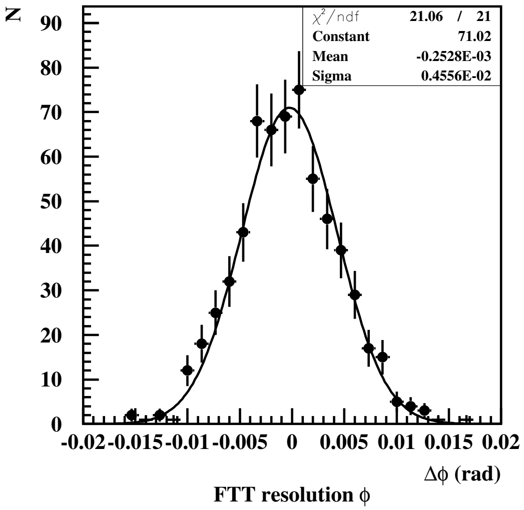
- Reconstruction of up to 48 tracks within 25 μsec
- Trigger efficiency of central tracks $\approx$ 95%

  for typical single hit detection efficiencies above 90%

- Track parameter resolution:

$$\frac{\sigma_{p_t}}{p_t} \approx \frac{0.04}{\mathrm{GeV}}$$





$\sigma_\Phi \approx$ 5 mrad

L3 Processing

Farm of Processor Boards identifies particle resonances, e.g.

- vector mesons

  $\rho \rightarrow \pi^+\pi^-, \quad \Phi \rightarrow K^+K^-$

  $J/\Psi,\ \Upsilon\ \rightarrow\ e^+e^-,\ \mu^+\mu^-$

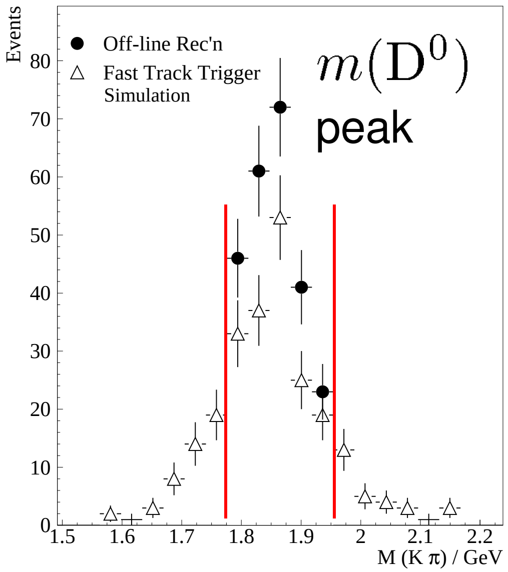
- *charm* and *bottom* $ep \rightarrow c\bar{c},\ b\bar{b}$ using:

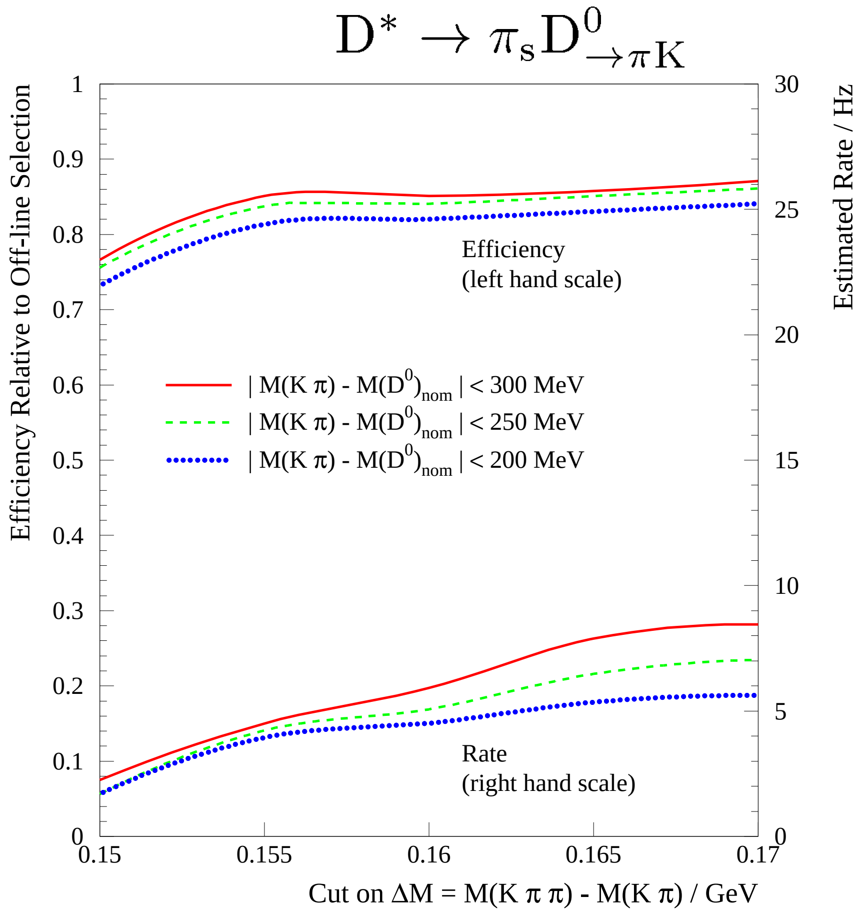
  D^*, D_s, D^+

  semi-leptonic decays

- Example:

  $D^* \rightarrow \pi_s D^0_{\rightarrow \pi K}$





Summary / Outlook

- Fast Track Trigger presented
  - 3-dimensional reconstruction of central tracks
  - selective: improving signal to background ratio up to a factor of 50 (D^* mesons)
  - flexible: multifunctional hardware components
  - reprogramable algorithms on DSPs, FPGAs, processor boards
  - expandable: vertex reconstruction, tracks from secondary vertices (not mentioned)
- Performance
  - fulfills trigger specifications in HERA environment
  - approaches offline reconstruction in precision
  - robust against severe running conditions
- FTT fully commissioned end of 2001