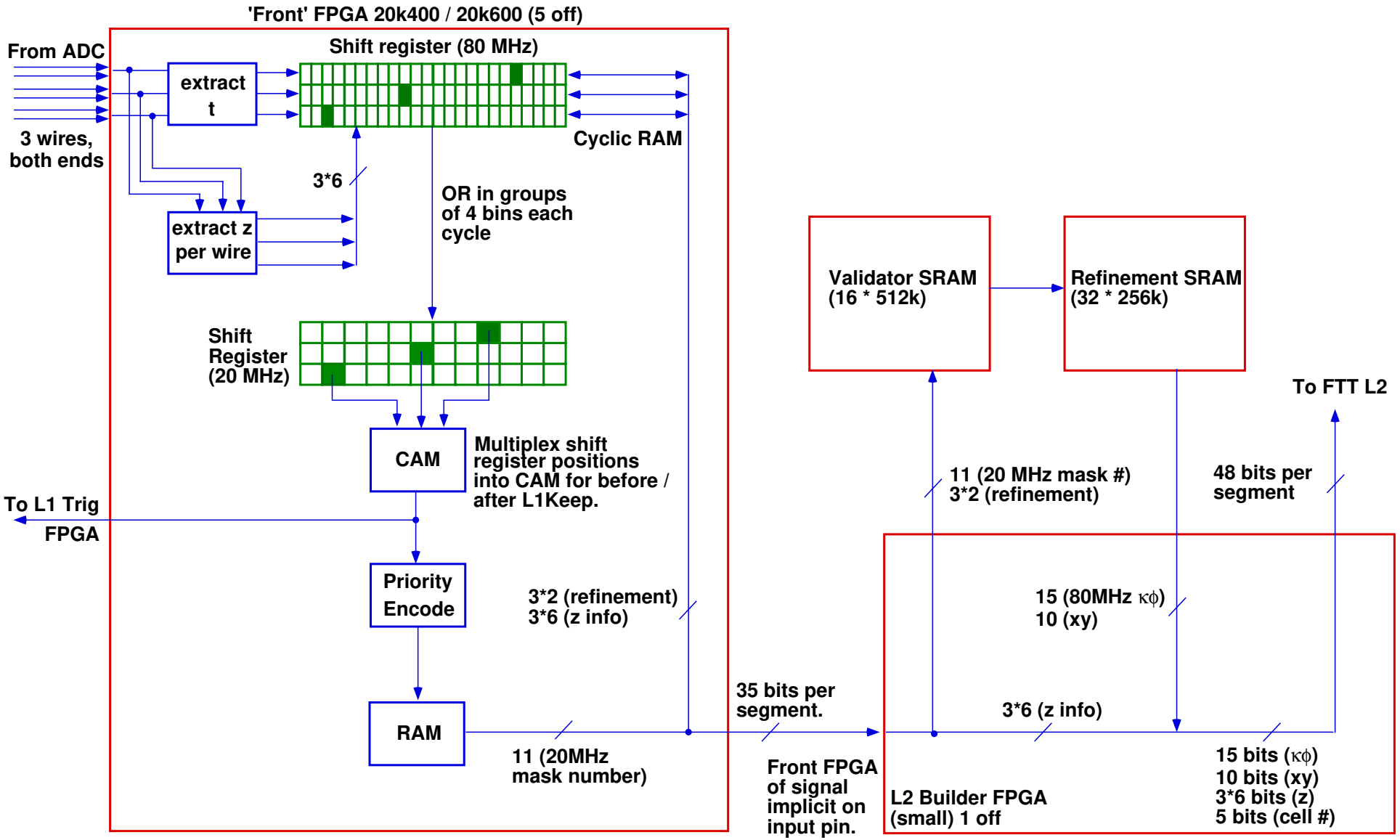
'Front' FPGA 20k400 / 20k600 (5 off)
From ADC
3 wires, both ends
extract t
Shift register (80 MHz)
Cyclic RAM
3*6
extract z per wire
OR in groups of 4 bins each cycle
Shift Register (20 MHz)
CAM
Multiplex shift register positions into CAM for before / after L1Keep.
To L1 Trig FPGA
Priority Encode
3*2 (refinement)
3*6 (z info)
RAM
11 (20MHz mask number)
35 bits per segment.
Front FPGA of signal implicit on input pin.
Validator SRAM (16 * 512k)
Refinement SRAM (32 * 256k)
To FTT L2
11 (20 MHz mask #)
3*2 (refinement)
48 bits per segment
15 (80MHz κϕ)
10 (xy)
3*6 (z info)
15 bits (κϕ)
10 bits (xy)
3*6 bits (z)
5 bits (cell #)
L2 Builder FPGA (small) 1 off