H1 FTT L1 deliverables and milestones

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The UK groups have undertaken the design and construction of the L1 part of the FTT, the L1 system, illustrated below and summarised in the table below as presented to the PPESP in January 2000. This L1 system digitises the analogue signals from the drift chamber, carries out in parallel the "*Q-t*" analysis and performs local track segment finding in fast FPGA arrays and the L1 trigger logic within 2.3 μs, before distributing the segment information appropriately for the later track linking and fitting in the L2 system.

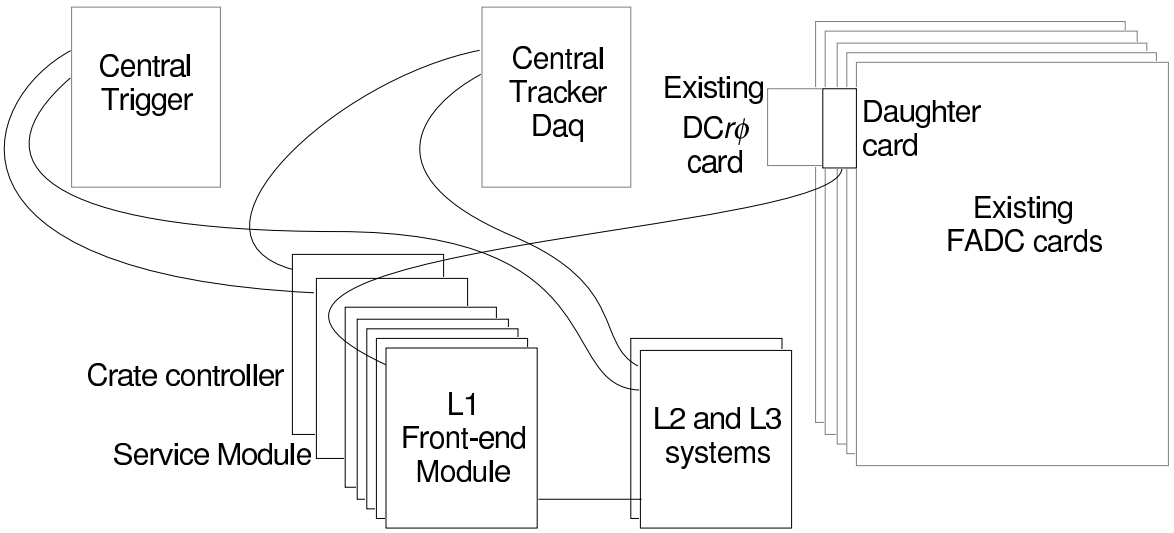

Figure 1 - Sketch of FTT hardware with L1 system highlighted and L2 and L3 systems in solid lines as proposed to PPESP.

Item	RAL ID	Other UK	Non-UK	Source of Effort
1. Analogue DC$r\phi$ Daughter Card		0.6		Manchester
2. a) L1 Front-end Module design	2.5			RAL ID
b) Coding *Q-t* algorithm		0.25		RAL PPD
c) Coding track segment finding algorithm		2.2	0.3	Birmingham/DESY
d) Integration into H1 and control			1	DESY
3. a) L1 service module/trigger card design		0.8		Manchester
b) Coding trigger algorithm		1		Birmingham
4. Trigger algorithms and simulation		1	1	Birmingham/DESY
5. Monitoring software		1.5		UK universities
6. System integration		0.5		UK universities
7. Project management		0.75		RAL PPD
Total	2.5	8.6	2.3	

Table 1 - Revised schedule in staff years for UK involvement in Fast Track Trigger project as presented to PPESP.

Since the proposal the project has evolved. In terms of the hardware the specification of items 1 and 2 above remain much as originally proposed, item 3 has split into separate service modules and possibly multiple L1 trigger cards, the latter subject to feasibility studies, and the back-plane bus will now be VME based. In terms of the software more emphasis within the UK is placed on providing the algorithm 2(c) and with the reduced RAL effort of 2.5 staff years compared to the requested 4 it is not obvious that items 5 and 6 are now covered.

Hardware Components

DC$r\phi$ Daughter Card

Hardware Description

Amplifies the signals from 6 of the 8 wires coming out the front panel DIN connector on an existing F1001 ADC card and passes these to the FEM. Also passes through the signals for 6 of the 8 wires to the existing DC$r\phi$ cards. Unfortunately there are at least two different sets of 6 wires required for the FEM and no doubt different sets for the DC$r\phi$ cards so probably at least 4 variants of this card need to be produced.

Interfaces

DIN connector into existing F1001 ADC card

DIN socket for existing DC$r\phi$ card

Socket for cable to FEM

Responsibility

Manchester

Time scales

Task	Delivery date
Design	before 09/00
Production	before 11/00
Installation	before 03/01

Table 2 - DC$r\phi$ daughter card time scales

Concerns

How many variants required

Power load on ADC crate - some crates are already on the limit with the existing DC$r\phi$ cards.

Front-End Module

Hardware Description

Takes signals from 5 groups (cells) of 6 wires (actually from both ends of 3 wires). Digitises these signals at 80 MHz (to match the later synchronisation frequency) to give fast timing information for local segment finding, with slower z determination by charge division.

Exchange information between neighbouring cells (including between adjacent modules in logical ring) to allow segment finding in cases where tracks cross cell boundaries.

Provide sufficient FPGA resource to allow at a minimum the Q-t digitisation and the local segment finding and refinement algorithm after L1KEEP and ideally also fast local segment finding in time to contribute to an L1 decision.

Pass refined segments to L2 system after L1KEEP, also have functionality to pass fast segment information to L1 trigger modules.

Interfaces

Input for cable from daughter card above - probably on front panel

Output for cable to L2 system - probably 14526-EZHB-200-0QC type cable and 10226-1210VE board connectors on front panel as suggested by SCS - but possibly by connection through back-plane

Interchange for 80 MHz information between adjacent modules in ring for segment finding via back-plane

Output of fast segment information (or $\kappa\phi$ histogram) to L1 trigger modules via back-plane

Minimal VME interface for downloading algorithm to FPGA, diagnostics and monitoring

Access to trigger signals

Responsibility

RAL as detailed below

Task	Staff months	Name
1. Analogue design	2	AB & DL
2. Digital design	4	AB & DL
3. PCB layout	6	BC
4. Debug	4	AB & DL & Technician
5. Firmware	4	DL
6. Production	4	Technician
7. Commissioning and installation	2	AB & DL
8. Control software	4	Real-time Systems Group
Total	30	

Table 3 - Detailed breakdown of effort from RAL Instrumentation Department for construction of the H1 Fast Track Trigger L1 Front-end Module. The key for names is AB - Adam Baird, DL - transfer from Daresbury (tbc) and BC - Brian Claxton.

Time scales

Task	Start	End
Preliminary design report	01/00	03/00
First design	03/00	06/00
Board layout	06/00	12/00
Prototype manufacture	12/00	01/01
Debug / testing prototype in isolation	01/01	03/01
Installation of prototype at H1		03/01
Redesign and layout	04/01	06/01
Main production	06/01	12/01

Table 4 - FEM time scales

Concerns

Delay

Not compatible with L2 prototypes available in October 2000

Controller Module

Hardware Description

Interfaces

Interface to H1 trigger signals and broadcast to FEMs

Interface to H1 Daq for monitoring and download of FPGA code

Responsibility

Manchester

Time scales

Concerns

L1 Trigger Module

Hardware Description

Interfaces

Trigger signals to H1 L1 Central Trigger logic

Connections from FEMs

Responsibility

Manchester/Birmingham

Time scales

Task	Start	End
L1 trigger viability determination	01/00	03/00
L1 trigger algorithm design	03/00	11/00
Design / layout of board		02/01
Prototype service module		03/01
Testing *in situ* at H1	04/01	11/01
Contingency for redesign of service module	06/01	09/01
Final production of service module		12/01

Table 5 - Trigger module time scales

Concerns

L1 Crate and Back-plane

Hardware Description

Basic VME back-plane on J1 connectors with a higher density connector on J2 to provide necessary interconnections between adjacent FEMs and also to the L1 Trigger modules

Interfaces

Basic VME on J1

Interconnect for FEMs and to L1 Trigger modules on J2, along with possible connections to L2 system on back

Responsibility

Manchester

Time scales

Concerns

Software Components

Q-t Algorithm

Software Description

Analyses the 80 MHz digitised data (to match the later synchronisation frequency) to give fast timing information for local segment finding, with slower *z* determination by charge division.

Responsibility

RAL PPD

Time scales

Task	Start	End
Testing and tuning algorithm using simulation & H1 data	01/00	04/00
VHDL for *Q-t* algorithm	04/00	10/00
FPGAs on prototypes programmed	10/00	03/01
Testing and tuning of algorithm *in situ* at H1	04/01	11/01

Table 6 - *Q-t* algorithm time scales

Concerns

z co-ordinate determination and its accuracy, especially in presence of synchrotron radiation hits

L2 Segment Finding and Refinement Algorithm

Software Description

Main segment finding does not begin until after L1KEEP, with data clocked through shift registers until then. Algorithm is based on a 20 MHz and 80 MHz segment finding using the frozen shift registers with the correct bunch crossing known *a priori*.

Responsibility

Birmingham and DESY (Zürich)

Time scales

Task	Start	End
Testing and tuning algorithm using simulation & H1 data	01/00	04/00
VHDL for segment finding algorithm	04/00	10/00
FPGAs on prototypes programmed	10/00	03/01
Testing and tuning of algorithm *in situ* at H1	04/01	11/01

Table 7- L2 segment finding algorithm time scales

Concerns

L1 Segment Finding Algorithm

Software Description

Algorithm based on patterns in the 20 MHz shift register, either using a pivot layer technique or serial assumptions of active bunch crossing, similar to L2 algorithm.

Responsibility

Birmingham

Time scales

Concerns

L1 Trigger Algorithm

Software Description

Responsibility

Birmingham

Time scales

Concerns

System Control Software

Software Description

Internal systems integration

Integration into H1 and control during running

Procurement and download of FPGA code

Monitoring

Responsibility

None as yet

Time scales

Task	Start	End
First version of software		03/01
Testing and redesigning control software	04/01	12/01

Table 8 - System control software time scales

Concerns

Above!